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(54) Title: COMPOSITE OPTICAL LITHOGRAPHY METHOD FOR PATTERNING LINES OF SIGNIFICANTLY DIFFERENT WIDTHS

(57) Abstract: A composite patterning technique may include three lithography processes. A first lithography process forms a periodic pattern of alternating continuous lines of substantially equal width and spaces on a first photoresist. A second lithography process uses a non-interference lithography technique to break continuity of the patterned lines and form portions of desired integrated circuit features. The first photoresist may be developed. A second photoresist is formed over the first photoresist. A third lithography process uses a non-interference lithography technique to expose a pattern on the second photoresist and form remaining desired features of an integrated circuit pattern.

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## COMPOSITE OPTICAL LITHOGRAPHY METHOD FOR PATTERNING LINES OF SIGNIFICANTLY DIFFERENT WIDTHS

### BACKGROUND

[0001] An integrated circuit (IC) manufacturing process  
5 may deposit various material layers on a wafer and form a  
photosensitive resist (photoresist) on the deposited layers.  
The process may use lithography to transmit light through or  
reflect light from a patterned reticle (mask) to the  
photoresist. Light from the reticle transfers a patterned  
10 image onto the photoresist. The process may remove portions  
of the photoresist which are exposed to light. A process  
may etch portions of the wafer which are not protected by  
the remaining photoresist to form integrated circuit  
features.

15 [0002] The semiconductor industry may continually strive  
to reduce the size of transistor features to increase  
transistor density and to improve transistor performance.  
This desire has driven a reduction in the wavelength of  
light used in photolithographic techniques to define smaller  
20 IC features in a photoresist. Complex lithographic exposure  
tools may cost more to make and operate.

### BRIEF DESCRIPTION OF DRAWINGS

[0003] Fig. 1A illustrates an interference lithography  
apparatus.

[0004] Fig. 1B illustrates an example of a diffraction grating with slits which allow light to pass through and radiate a photoresist on a substrate.

[0005] Fig. 2 illustrates a latent or real image of an interference pattern of spaces and lines produced by the interference lithography apparatus of Fig. 1A or Fig. 1B.

[0006] Fig. 3A illustrates a desired final layout of lines with significantly different widths formed by first, second and third lithography processes.

10 [0007] Fig. 3B illustrates a layout after the latent pattern of continuous, non-exposed lines and exposed spaces of Fig. 2 has been altered by a second lithography process.

[0008] Fig. 3C shows an approximate exposed layout of the second lithography process mask or its corresponding database for maskless patterning.

[0009] Fig. 3D shows a corresponding layout of a second mask used by a third lithography process.

[0010] Figs. 4A-4H illustrate an example of a second lithography process to expose areas on a photoresist and subsequent processes of developing, etching and stripping.

20 [0011] Fig. 5 illustrates a composite optical lithography exposure system with a movable wafer stage.

[0012] Fig. 6 shows an optical lithographic implementation of the second patterning system.

[0013] Fig. 7 is flow chart of a composite lithography patterning technique.

[0014] Fig. 8 shows a process for generating a layout of a mask for the second lithography process.

5 [0015] Fig. 9 shows an example of a design layout.

[0016] Fig. 10 shows an example of a remainder layout.

[0017] Fig. 11 shows a remainder layout after an expansion in a direction D.

#### DETAILED DESCRIPTION

10 [0018] A conventional patterning technique may use expensive, diffraction-limited, high numerical aperture (NA), high aberration-corrected lens or tools equipped with complex illumination. A conventional patterning technique may also use complicated and expensive masks, which employ  
15 various phase shifters and complex optical proximity corrections (OPC).

[0019] The present application relates to a composite optical lithography patterning technique, which may form smaller integrated circuit features compared to conventional  
20 lithography techniques. The composite patterning technique may provide a higher density of integrated circuit features for a given area on a substrate.

[0020] The composite patterning technique may include two or more lithography processes. A first lithography process

may use interference lithography to form a periodic alternating pattern of lines of substantially equal width and spaces on a first photoresist. A second lithography process may use a non-interference lithography technique to  
5 break continuity of the patterned lines formed by the first lithography process and remove resist over layout area where features of substantially larger width would need to be patterned. The first photoresist may be developed, and a second photoresist may be formed. A third lithography may  
10 expose features with significantly larger widths than the interference pattern line width.

[0021] The composite patterning technique may form patterns of lines with significantly different widths. For example, one line width may be 10% greater than another line  
15 width. As another example, one line width may be more than 30% greater than another line width. Patterned lines with significantly different widths may be desirable in integrated circuit (IC) manufacturing, for example, to pattern gates with significantly different widths. Gates  
20 with significantly different widths may optimize speed and/or power performance of an integrated circuit.

[0022] In another embodiment, the first process may include a non-interference lithography technique, and the second process may include an interference lithography  
25 technique.

**[0023]     First Lithography Process**

[0024]     Fig. 1A illustrates an interference (interferometric) lithography apparatus 100. The interference lithography apparatus 100 may include a beam splitter 104 and two mirrors 106A, 106B. The beam splitter 104 may receive radiation, such as a conditioned (expanded and collimated) laser beam 102, from a radiation source with a pre-determined exposure wavelength ( $\lambda$ ). The beam splitter 104 may direct the radiation 102 to the mirrors 106A, 106B. The mirrors 106A, 106B may form an interference pattern 200 (Fig. 2) on a substrate 108 with a photosensitive media, such as a photoresist layer 107. Many interferometric lithography tool designs with various complexity and sophistication are available. Either a positive or a negative photoresist may be used with the processes described herein.  $\theta$  may be an angle between a surface normal of the photoresist 107 and a beam of radiation incident on the photoresist 107.

[0025]     Fig. 2 illustrates a latent or real image of an interference pattern 200 of spaces 204 (exposed to light) and lines 202 (not exposed to light) produced by the interference lithography apparatus 100 of Fig. 1A. "Latent" refers to a pattern on the photoresist 107 which experienced a chemical reaction due to radiation but has not yet been developed in a solution to remove the exposed areas of the

positive tone photoresist 107 (Fig. 4C described below).

The lines 202 may have a substantially equal width. The spaces 204 may or may not have a width equal to the width of the lines 202.

5 [0026] "Pitch" is a sum of a line width and a space width in Fig. 2. As known to those of ordinary skill in optics, a "minimal pitch," which can be resolved by a projection optical exposure apparatus with a pre-determined wavelength  $\lambda$  and numerical aperture NA, may be expressed as:

10 [0027]  $\text{pitch}/2 = (k_1(\lambda/n_i))/\text{NA}$ ,

where "NA" is the numerical aperture of a projection lens in the lithography tool, and " $n_i$ " is the refractive index of a media between the substrate 108 and the last element of the optical projection system, e.g., mirrors 106A, 106B.

15 Optical projection systems currently in use for microlithography use air, which has  $n_i = 1$ . For liquid immersion microlithographic systems,  $n_i > 1.4$ . For  $n_i = 1$ , the pitch may be expressed as:

[0028]  $\text{pitch}/2 = k_1\lambda/\text{NA}$

20 [0029]  $\text{pitch} = 2k_1\lambda/\text{NA}$

[0030] where  $k_1$  is known as Rayleigh's constant. "NA" may be expressed as:

[0031]  $\text{NA} = n_0\sin\theta$ .

[0032] NA may be equal to 1.

[0033] If  $k_1 = 0.25$ , and  $n_0$  is about equal to one, pitch may expressed as:

[0034]  $\text{pitch} = 2(.25)\lambda/n_0\sin\theta \cong \lambda/2\sin\theta$

[0035] Other values of  $k_1$  may be greater than 0.25.

5 [0036] The interference lithography apparatus 100 of Fig. 1A may achieve a "minimal pitch" (a minimal line width plus space width) expressed as:

[0037]  $\text{minimal pitch} \cong \lambda/2$

[0038] The lines 202 and spaces 204 may have a pitch  $P_1$   
10 approaching  $\lambda_1/2$ , where  $\lambda_1$  is the radiation wavelength used in the interference lithography process. The wavelength  $\lambda_1$  may equal to 193 nm, 157 nm or an extreme ultraviolet (EUV) wavelength, such as 11-15 nm. Larger pitches may be obtained by changing the angle  $\theta$  of interfering beams in  
15 Fig. 1A.

[0039] Minimal feature size of an exposed space 204 or non-exposed line 202 may be equal to, less than or larger than exposure wavelength divided by four ( $\lambda/4$ ).

[0040] The first (interference lithography) process may  
20 define a width of all minimal critical features of a final pattern at a maximum density achievable by means of optical patterning with maximum process latitude.

[0041] Instead of the beam splitter 104, any light-splitting element may be used, such as a prism or



diffraction grating, to produce a pattern 200 of alternating lines 202 and spaces 204 on the photoresist 107.

[0042] Fig. 1B illustrates an example of a diffraction grating 120 with slits 122 which allow light to pass through and radiate a photoresist 107 on a substrate 108. The diffraction grating 120 in conjunction with projection optics may produce the same interference pattern 200 (Fig. 2) as the beam splitter 104 and mirrors 106A, 106B of Fig. 1A.

[0043] The size of the interference pattern 200 formed by interference lithography may be equal to a die, multiple dies or a whole wafer, e.g., a 300-mm wafer or even larger future generation wafer sizes. Interference lithography may have excellent dimensional control of an interference pattern 200 due to a large depth of focus.

[0044] Interference lithography may have a lower resolution limit and better dimensional control than lens-based lithography. Interference lithography may have a higher process margin than lens-based lithography because depth of focus for interference lithography may be hundreds or thousands of microns, in contrast to a fraction of a micron (e.g., 0.3 micron) depth of focus for some conventional lithography techniques. Depth of focus may be important in lithography since a photoresist may not be completely flat since (a) the photoresist is formed over one

or more metal layers and dielectric layers or (b)  
semiconductor wafer itself might not be sufficiently flat.

[0045] An embodiment of interference lithography may not  
need a complicated illuminator, expensive lenses, projection  
5 and illumination optics or a complex mask, in contrast to  
other lithography techniques.

[0046] Second Lithography Process

[0047] A second lithography process may include one or  
more non-interference lithography techniques, such as a  
10 conventional lithography technique, such as optical  
lithography, imprint lithography and electron-beam (e-beam)  
lithography. The second lithography process may use a mask  
(or reticle), as described below with reference to Figs. 3C  
and 4B. The second lithography process may use a "trim"  
15 mask technique, another mask-based technique or a maskless  
patterning technique. The second lithography process may  
use extreme ultraviolet (EUV) lithography.

[0048] The second lithography process may remove unwanted  
portions of lines 202 with minimal line width  $W_1$  of the  
20 pattern formed by the first lithography process.

[0049] Fig. 3A illustrates an example of a desired layout  
300 of lines 202, 310 with significantly different widths  $W_1$ ,  
 $W_4$  and  $W_5$  formed by the interference lithography process  
described above and second and third lithography processes  
25 described below.  $W_4$  is a line that connects two other lines

202 which are oriented orthogonally to W4. So "width" of W4 is orthogonal to width of those lines 202. The difference in layout and widths  $W_1$ ,  $W_4$ ,  $W_5$  in Fig. 3A may be exaggerated for illustrative purposes.

5 [0050] Fig. 3B illustrates a layout 320 after the latent pattern 200 of continuous, non-exposed lines 202 and exposed spaces 204 of Fig. 2 (formed on the photoresist 107 by the interference lithography process) has been altered by a second lithography process. The second lithography process  
10 exposes areas 318A-318C, which expose (remove) portions of the non-exposed continuous lines 202 formed in a positive photoresist. The non-exposed lines 202 formed by the interference lithography process have a width  $W_1$ , which may be the width of a narrowest desired line 202 in Fig. 3A.  
15 Width  $W_1$  is narrower than widths  $W_2$ ,  $W_3$  and  $W_5$  of area 318A-318C (Fig. 3B) exposed to radiation by the second lithography process. The second lithography process may expose a large section 318C which exposes several lines 202 (Fig. 2) of the pattern 200.

20 [0051] The second lithography process breaks continuity and regularity of periodic alternating continuous lines 202 and space 204 produced in the first lithography process.

[0052] The pattern layout of the second lithography process' exposure mask 330 in Fig. 3C (or maskless  
25 patterning tool database) may be a Boolean difference

between (a) a desired final pattern, such as the layout 300 in Fig. 3A, and (b) the pattern 200 (Fig. 2) formed by the interference lithography process. An approximate exposed layout of the second process' mask 330 (or its corresponding database for maskless patterning) is shown in Fig. 3C. Fig. 3C shows transparent regions 318A-318C in an opaque mask 330. The transparent regions 318A-318C expose radiation through the mask 330 if patterning of the second processing is produced by means of projection optical lithography for a positive resist. Thus, the spaces 204 and areas 318A-318C in Fig. 3B are exposed to radiation during the first and second lithography positive resist processes, respectively.

[0053] In an embodiment, the minimal pitch  $P_2$  (Fig. 3C) of the second lithography process may be 1.5 times the size of the minimal pitch  $P_1$  ( $\lambda_1/2$ ) of the interference lithography process described above. Thus,  $P_2 = 1.5(P_1) = 1.5(\lambda_1/2) = 0.75\lambda_1$ .

[0054] Fig. 7 is flow chart of a composite lithography patterning technique. At 700, an interference lithography process (described above), or a conventional lithography process employing an alternating phase shifted mask, forms the latent image pattern 200 (Fig. 2) of periodic continuous alternating lines 202 and spaces 204 on a first photoresist 107 with a minimal pitch approaching a resolution limit of optical imaging ( $k_1 = 0.25$ ). A second lithography process

exposes portions of the non-exposed lines 202 to form areas 318A-318C (Fig. 3B) at 702. After the second lithography exposure is complete, the first photoresist 107 may be developed at 704, as described below with reference to Fig.

5 4C.

[0055] A second photoresist may be applied over the first photoresist 107 (used by the first and second lithography processes) at 706. The second photoresist may be chemically different (distinct) from the first photoresist 107. The  
10 chemically different first and second photoresists may (a) prevent mixing of the photoresists and (b) enable chemically selective development of portions of the second photoresist exposed by a third lithography process without affecting the pattern formed in the first photoresist 107 by the first and  
15 second lithography processes.

[0056] Alternatively, the second photoresist may be the same chemically as the first photoresist but receive different processing.

[0057] Alternatively, a layer of  $\lambda_1$  radiation absorbing  
20 organic or inorganic film may be deposited in between the first and second photoresists to prevent mixing of the first and second resists and prevent exposure of the first resist lines 202 to the third lithography process' radiation.

[0058] A third lithography exposure process at 708 may  
25 pattern features 310 (Figs. 3A and 3D) with line widths  $W_4$ ,

$W_5$  that are significantly larger than features patterned during the first and second lithography processes. The third lithography exposure process may use a conventional lithography technique, as described above. The third  
5 lithography process may use a second mask (or database) and optics to form a pattern which has a larger pitch than the second lithography process pattern. The third lithography process may use the same apparatus as the second lithography process but with a different mask or database.

10 [0059] Fig. 3D shows a corresponding layout of a second mask used by the third lithography process. If a positive resist is used for the third lithography process, large features 310 in Fig. 3D with widths  $W_4$  and  $W_5$  of the second mask are oblique features on a transparent mask 340.

15 Tonality of mask and features are reversed if a negative resist is used for the third lithography process.

[0060] A database for the second mask used in the third lithography process may contain only "large" lines  $W_4$ ,  $W_5$  (Fig. 3A) present in the original layout database which are  
20 sized to accommodate processing steps overlay requirements and mask making processing specificity known in the art of patterning.

[0061] The second photoresist may be developed at 710, which results in a final layout 300 (Fig. 3A) in the two  
25 photoresists. The substrate 108 and patterned photoresists

are ready for subsequent processes in an IC process flow, such as etching (Fig. 4D), at 712.

[0062] Figs. 4A-4H illustrate an example of a second lithography process to expose areas 320 (Fig. 3C) on the photoresist 107 and subsequent processes of developing, etching and stripping. A photoresist 107 may be formed (e.g., coated) on a substrate 108 in Fig. 4A. A latent or real interference pattern 200 (Fig. 2) may be formed on the photoresist 107 by the interference lithography apparatus 100 of Fig. 1A. A second lithography tool (second lithography process) may transmit light 403 through a patterned mask or reticle 404 to expose desired areas 302 of the photoresist 107 in Fig. 4B. The light 403 may start a reaction in the exposed areas 320. The light 403 may be ultraviolet, deep ultraviolet or extreme ultraviolet (EUV) radiation, for example, with a wavelength of about 11-15 nanometers (nm).

[0063] The photoresist 107 and substrate 108 may be removed from the lithography tool and baked in a temperature-controlled environment. Radiation exposure and baking may change the solubility of the exposed areas 320 and spaces 204 (Fig. 2) compared to unexposed areas of the photoresist 107.

[0064] The photoresist 107 may be "developed," i.e., put in a developer and subjected to an aqueous (H<sub>2</sub>O) based

solution, to remove exposed areas 320 and spaces 204 of the photoresist 107 in Fig. 4C to form a desired pattern in the resist. If a "positive" photoresist is used, exposed areas 320 and spaces 204 may be removed by the solution. Portions 5 410 of the substrate 108 which are not protected by the remaining photoresist 107 may be etched in Fig. 4D to form desired circuit features. The remaining photoresist 107 may be stripped in Fig. 4E. If a "negative" photoresist is used, areas which are not exposed to radiation may be 10 removed by the developing solution, as shown in Fig. 4F. Then portions 420 of the substrate 108 which are not protected by the remaining photoresist 422 may be etched in Fig. 4G to form desired circuit features. The remaining photoresist 422 may be stripped in Fig. 4H.

15 [0065] Combining an interference lithography technique and a non-interference lithography technique may provide high IC pattern density scaling (patterning at  $k_1 = 0.25$  for any available wavelength).

[0066] Interference lithography, which patterns minimal 20 pitch features, may extend 193-nm immersion lithography to 66-nm pitch and may extend an EUV interference tool capability down to 6.7-nm pitch.

[0067] Interference lithography may have an all-reflective design, e.g., Lloyds' mirror interferometric 25 lithographic system, which may enable system design with



available wavelengths between 157 nm and 13.4 nm, such as a neon discharge source (about 74-nm wavelength) and a helium discharge source (58.4-nm wavelength) with corresponding minimal pitches of 37 nm and 30 nm, respectively.

5 [0068] The second lithography process may be preceded by applying another layer of patterning media. The selected second lithography process may determine which patterning media is selected.

[0069] Alignment

10 [0070] An existing alignment sensor on the interference lithography apparatus 100 may align the pattern 200 (Fig. 2) produced by the first lithography process to a previous layer pattern formed by other processes. An existing alignment sensor may be above a wafer and be adapted to  
15 sense a mark on the wafer.

[0071] Alignment of the second and fourth lithography process to the first lithography process may be achieved by either indirect alignment (second lithography process patterning aligns to previous layer pattern by means of  
20 existing alignment sensors) or direct alignment (second lithography process patterning aligns to first lithography process pattern 200 directly) by means of a latent image alignment sensor.

[0072] Fig. 5 illustrates a composite optical lithography  
25 system 500 with a movable wafer stage 545. The composite

optical lithography system 500 may include an environmental enclosure 505, such as a clean room or other location suitable for printing features on substrates. The enclosure 505 encloses an interference lithography system 510 and a  
5 second (non-interference) patterning system 515. The interference lithography system 510 may include a collimated radiation source 520 and interference optics 525 to provide interferometric patterning on a photoresist.

[0073] The second patterning system 515 may use one of  
10 several techniques to pattern a photoresist. For example, the second patterning system 515 may be an e-beam projection system, an imprint printing system, or an optical lithography system. Alternatively, the second patterning system 515 may be a maskless module, such as an electron  
15 beam direct write module, an ion beam direct write module, or an optical direct write module.

[0074] The two systems 510, 515 may share a common mask handling subsystem 530, a common wafer handling subsystem 535, a common control subsystem 540, and a common stage 545.  
20 The mask handling subsystem 530 may position a mask in the system 500. The wafer handling subsystem 535 may position a wafer 561 in the system 500. The control subsystem 540 may regulate one or more properties or devices of system 500 over time. For example, the control subsystem 540 may  
25 regulate the position, alignment or operation of a device in

system 500. The control subsystem 540 may also regulate a radiation dose, focus, temperature or other environmental qualities within environmental enclosure 505.

[0075] The control subsystem 540 can also translate the  
5 stage 545 between a first exposure stage position 555 and a second exposure stage position 550. The stage 545 includes a wafer chuck 560 for gripping a wafer 561. At the first position 555, the stage 545 and the chuck 560 may present a gripped wafer 561 to the interference lithography system 510  
10 for interferometric patterning. At the second position 550, the stage 545 and the chuck 560 may present the gripped wafer 561 to the second patterning system 515 for patterning.

[0076] To ensure the proper positioning of a wafer 561 by  
15 the chuck 560 and the stage 545, the control subsystem 540 may include an alignment sensor 565. The alignment sensor 565 may transduce and control the position of the wafer 561 (e.g., using wafer alignment marks) to align a pattern formed by the second patterning system 515 with a pattern  
20 formed by the interference lithography system 510. Such positioning may be used when introducing irregularity into a repeating array of interferometric features, as discussed above.

[0077] Fig. 6 shows an optical lithographic  
25 implementation of the second patterning system 515. In

particular, the second patterning system 515 may be a step-and-repeat projection system. Such a patterning system 515 may include an illuminator 605, a mask stage 610, a mask 630 and projection optics 615. The illuminator 605 may include  
5 a radiation source 620 and an aperture/condenser 625. The radiation source 620 may be the same as radiation source 520 in Fig. 5. Alternatively, the radiation source 620 may be a separate device. The radiation source 620 may emit radiation at the same or at a different wavelength as the  
10 radiation source 520.

[0078] The aperture/condenser 625 may include one or more devices for collecting, collimating, filtering, and focusing the emitted radiation from the radiation source 520 to increase the uniformity of illumination upon mask stage 610.  
15 The mask stage 610 may support a mask 630 in the illumination path. The projection optics 615 may reduce image size. The projection optics 615 may include a filtering projection lens. As the stage 545 translates a gripped wafer 561 for exposure by the illuminator 605  
20 through mask stage 610 and projection optics 615, the alignment sensor 565 may ensure that the exposures are aligned with a repeating array 200 of interferometric features to introduce irregularity into the repeating array 200.

[0079] Fig. 8 shows a process 800 for generating a layout of a mask for the second lithography process described above.

The process 800 may be performed by one or more actors (such as a device manufacturer, a mask manufacturer, or a foundry)

5 acting alone or in concert. The process 800 may also be performed in whole or in part by a data processing device executing a set of machine-readable instructions.

[0080] The actor performing the process 800 receives a design layout at 805. The design layout is an intended

10 physical design of a layout piece or substrate after processing. Figs. 3A and 9 show examples of such design layouts 300, 900. The design layout 300, 900 may be received in a machine-readable form. The physical design of the layout 300, 900 may include a collection of trenches and

15 lands between the trenches. The trenches and lands may be linear and parallel. The trenches and lands need not repeat regularly across the entire layout piece. For example, the continuity of one or both of trenches and lands may be cut at arbitrary positions in the layout 300, 900.

20 [0081] Returning to Fig. 8, the actor performing the process 800 may also receive a pattern array layout 200 of alternating, parallel lines 202 and spaces 204 (Fig. 2) at 810. The pattern array layout 200 may be formed on a photoresist 107 by interferometric lithography techniques,

i.e., interference of radiation. The pattern array layout 200 may be received in a machine-readable form.

[0082] Returning to Fig. 8, the actor may subtract the design layout 900 (Fig. 9) from the pattern array layout 200 (Fig. 2) at 815. The subtraction of the design layout 900 from the pattern array layout 200 may include aligning trenches 332 in the design layout 900 with either lines or spaces in the pattern array layout 200 and determining positions where irregularity in the design layout 900 prevents complete overlap with the pattern array layout 200.

[0083] Figs. 3C and 10 show examples of remainder layouts 330, 1000 that indicate positions where the design layouts 300, 900 do not completely overlap with the pattern array layout 200 (Fig. 2). The remainder layouts 330, 1000 may be in machine-readable form. The subtraction may be Boolean because positions in the remainder layouts 330, 1000 may have only one of two possible states. In particular, the remainder layout 1000 includes expanses of first positions 1005 with a "not overlapped" state and a contiguous expanse of second positions 1010 with an "overlapped" state.

[0084] Returning to Fig. 8, the actor may resize expanses of positions in the remainder layout 1000 at 820. The resizing of the remainder layout 1000 may result in a changed machine-readable remainder layout 1100 in Fig. 11. Fig. 11 shows a remainder layout 1100 after such an expansion in a

direction D. When the pattern array is an array 200 of parallel lines 202 and spaces 204, the size of expanses 1105 with a present state may be increased in the direction perpendicular to the lines 202 and spaces 204. Some  
5 expanses 1105 may merge.

[0085] Returning to Fig. 8, the actor may generate a print mask using the remainder layout 1000 in Fig. 10 at 825. The print mask may be generated using the resized remainder layout 1100 of Fig. 11 to create arbitrarily shaped features  
10 for introducing irregularity into a repeating array, such as the pattern array 200 (Fig. 2). The generation of the print mask may include generating a machine-readable description of the print mask. The generation of the print mask may also include tangibly embodying the print mask in a mask  
15 substrate.

[0086] Alternatively, if the second lithography process uses EUV wavelengths, elements of an EUV lithography system, including the mask to be used, may be reflective. The clear (transmissive) areas on a non-EUV mask will be reflective  
20 areas on a EUV mask, and opaque (chrome) areas on a non-EUV mask will be absorptive areas on an EUV mask.

[0087] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit

and scope of the application. Accordingly, other embodiments are within the scope of the following claims.



**WHAT IS CLAIMED IS:**

1. A system comprising:

a first apparatus to radiate a periodic pattern of alternating non-exposed lines and exposed spaces on a first photoresist, the lines having a substantially equal first width; and

a second apparatus to expose a portion of at least one line to radiation to form a feature with a second width, the second width being larger than the first width of the lines, the second apparatus to radiate an area of a second photoresist over the first photoresist, the area having a third width.

2. The system of Claim 2, wherein a pitch of a pattern produced by the second apparatus is greater than or equal to one and a half times a minimal pitch of the periodic pattern of alternating lines and spaces.

3. The system of Claim 1, wherein the second photoresist is chemically distinct from the first photoresist.

4. The system of Claim 1, wherein the first apparatus comprises a beamsplitter.

5. The system of Claim 1, wherein the first apparatus comprises a diffraction grating.

6. The system of Claim 1, wherein the first apparatus  
5 comprises a optical projection lithography tool using an alternating phase shifter mask.

7. The system of Claim 1, wherein the second apparatus comprises a mask-based optical lithography tool.

10

8. The system of Claim 1, wherein the second apparatus comprises a maskless optical lithography tool with a database.

15

9. The system of Claim 1, wherein the second apparatus comprises an imprint lithography tool.

10. The system of Claim 1, wherein the second apparatus comprises an imprint electron beam tool.

20

11. A method comprising:

radiating a periodic pattern of alternating non-exposed lines and exposed spaces on a first photoresist, the lines having a first width; exposing a portion of at least one  
25 line to radiation to break continuity of the line and

regularity of pattern and form a feature with a second width, the second width being greater than the first width;

developing the first photoresist;

forming a second photoresist over the first

5 photoresist; and

radiating an area of the second photoresist, the area having a third width.

12. The method of Claim 11, wherein a pitch of the  
10 feature is greater than or equal to one and a half times a pitch of the interference pattern.

13. The method of Claim 11, wherein the radiation has a wavelength, the alternating pattern of lines and spaces  
15 having a pitch equal to about the wavelength divided by two.

14. The method of Claim 11, wherein the second photoresist is chemically distinct from the first photoresist.

20

15. The method of Claim 11, wherein the second photoresist is separated from first photoresist by means of third barrier layer residing between the first and second photoresists, the barrier layer having a property of  
25 sufficiently high absorption of light to expose the first

photoresist and a chemical structure that prevents mixing of the first and second photoresists.

16. The method of Claim 11, further comprising  
5 aligning the feature to the interference pattern.

17. The method of Claim 11, further comprising  
aligning the area to the feature.

10 18. The method of Claim 11, further comprising  
generating a print mask from subtraction of (a) a final  
design layout for a given layer from (b) the interference  
pattern.

15 19. An apparatus comprising:  
a first patterning apparatus including an interference  
exposure module to produce a first exposure of spaces and  
lines on a photoresist;

a second patterning apparatus to produce a second  
20 exposure, the second exposure reducing regularity of the  
first exposure; and

a third patterning apparatus to produce a third  
exposure on a second photoresist over the first photoresist,  
the third exposure exposing areas wider than features of the  
25 second exposure.

20. The apparatus of Claim 19, further comprising an alignment sensor to align the second exposure to the first exposure formed.

5

21. The apparatus of Claim 19, further comprising a common control system to move the first photoresist in a first position for the interference exposure module and in a second position for the second patterning module.

10

22. The apparatus of Claim 19, where the interference exposure module comprises an interference lithography module, and the second patterning module comprises a projection optical lithography system, the projection  
15 optical lithography system comprising projection optics, a wafer stage, and a mask to reduce regularity in the first exposure created by the interference exposure module.

23. The apparatus of Claim 19, where the interference  
20 exposure module comprises an interference lithography module, and the second patterning module comprises an imprint system that comprises projection optics, a wafer stage, and a mask to reduce regularity in the first exposure created by the interference exposure module.

25

24. The apparatus of Claim 19, where the interference exposure module comprises an interference lithography module, and the second patterning module comprises an electron projection system that comprises projection optics,  
5 a wafer stage, and a mask to reduce regularity in the first exposure created by the interference exposure module.

25. The apparatus of Claim 19, where the interference exposure module comprises an interference lithography  
10 module, and the second patterning module comprises a maskless module to reduce regularity in the first exposure created by the interference exposure module, projection optics and a wafer stage.

15 26. The apparatus of Claim 25, wherein the maskless module comprises an optical direct write module.

27. The apparatus of Claim 25, wherein the maskless module comprises an electron beam direct write module.

20

28. The apparatus of Claim 25, wherein the maskless module comprises an ion beam direct write module.

29. The apparatus of Claim 19, where the interference  
25 exposure module comprises an interference lithography

module, and the second patterning module comprises an X-ray proximity projection system that contains a mask to reduce regularity in a pattern created by the interference exposure module, projection optics and a wafer stage.

5

30. A method comprising:

receiving a pre-determined design layout;

receiving a pattern layout of alternating, parallel lines and spaces; and

10 subtracting the design layout from the pattern layout of alternating, parallel lines and spaces to form a remainder layout.

31. The method of Claim 30, further comprising

15 aligning features of the design layout with at least one of the lines and spaces of the pattern layout.

32. The method of Claim 30, further comprising

generating a machine-readable description of a print mask  
20 with the remainder layout.

33. The method of Claim 30, further comprising

generating a print mask with the remainder layout.

34. The method of Claim 30, further comprising  
resizing features of the remainder layout.



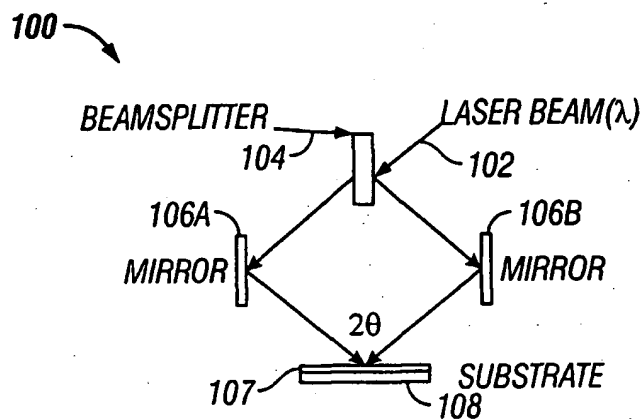


FIG. 1A

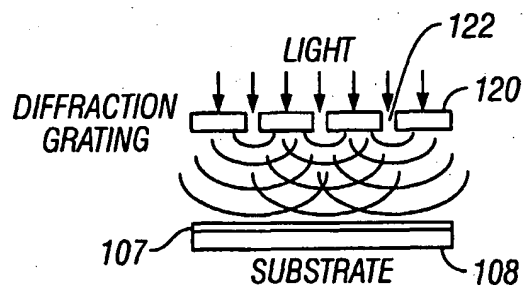


FIG. 1B

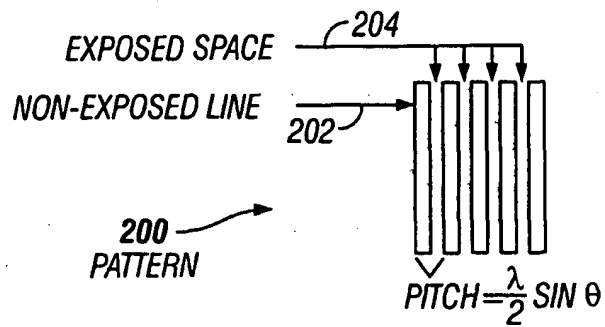


FIG. 2

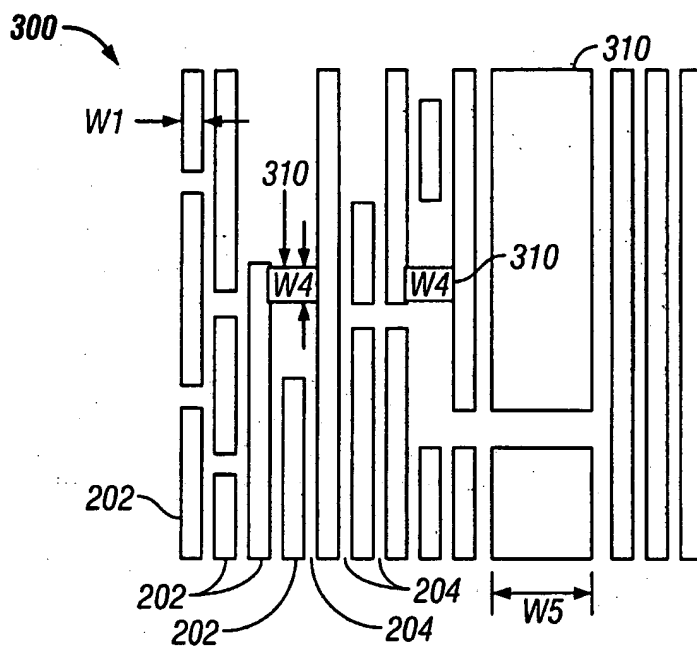


FIG. 3A

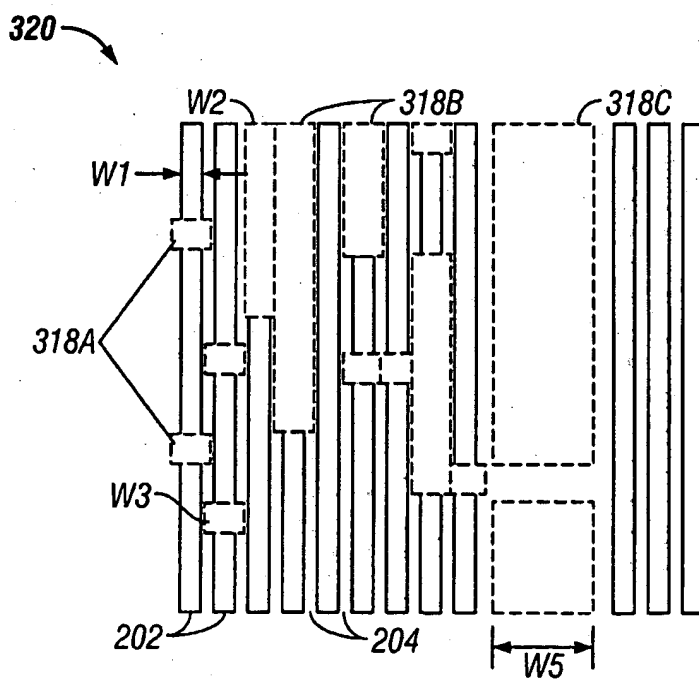


FIG. 3B

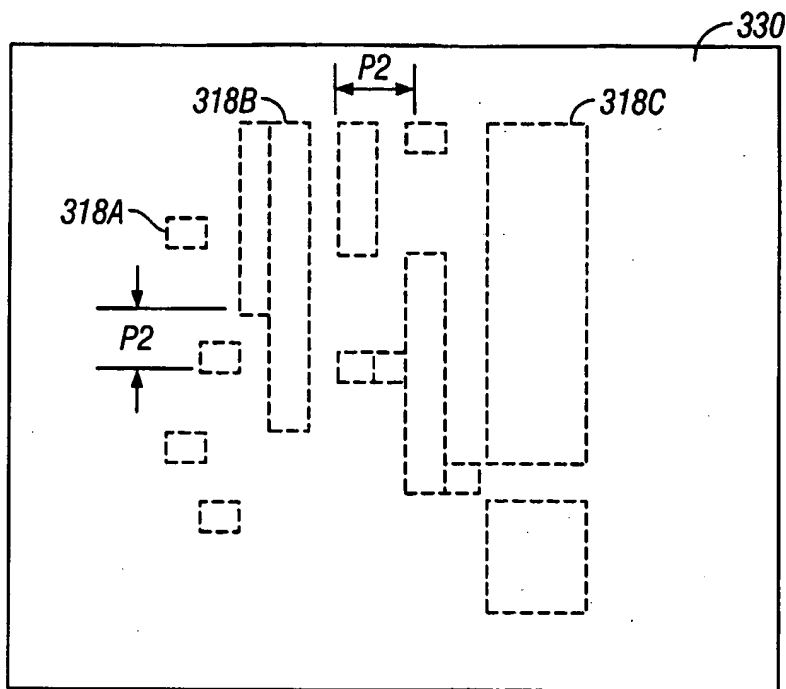


FIG. 3C

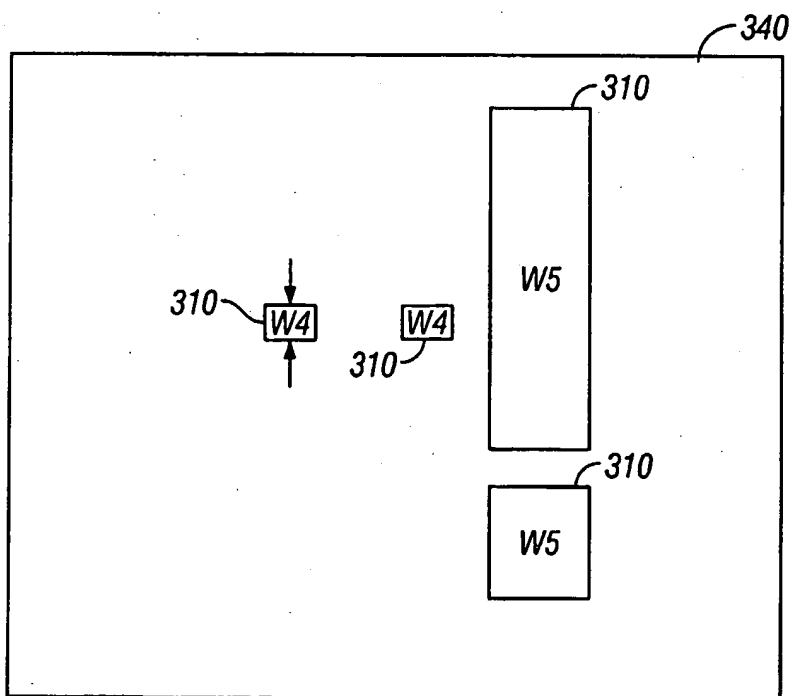


FIG. 3D

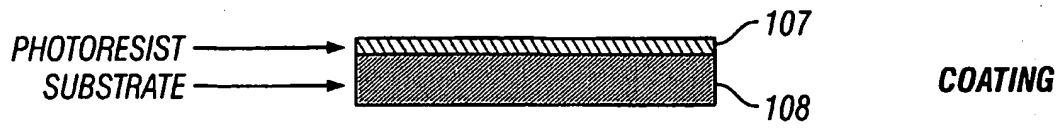


FIG. 4A

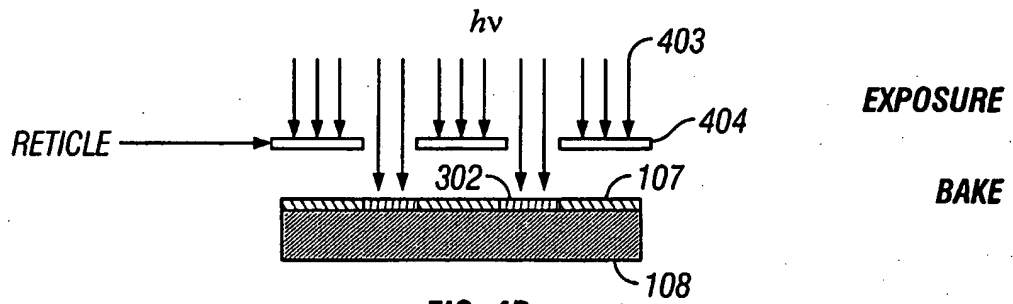


FIG. 4B

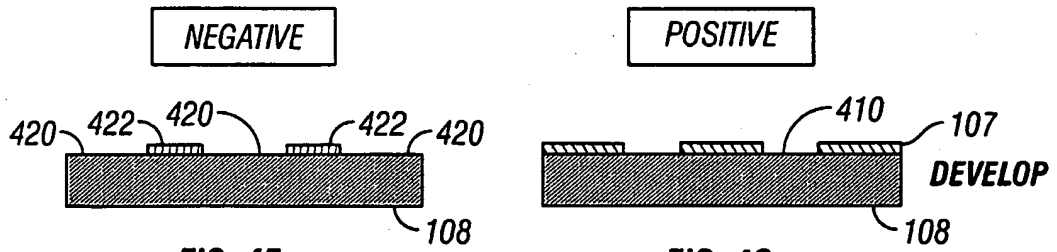


FIG. 4F

FIG. 4C

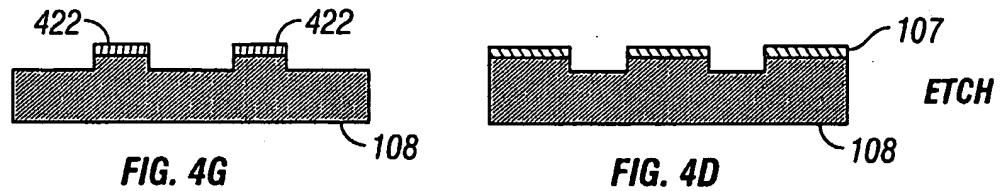


FIG. 4G

FIG. 4D

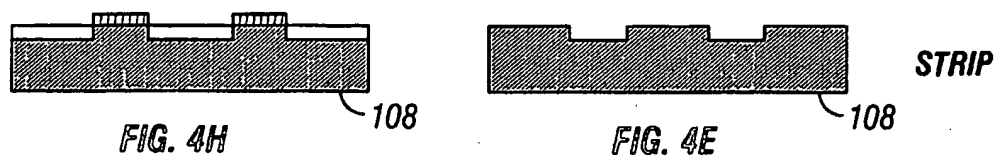


FIG. 4H

FIG. 4E

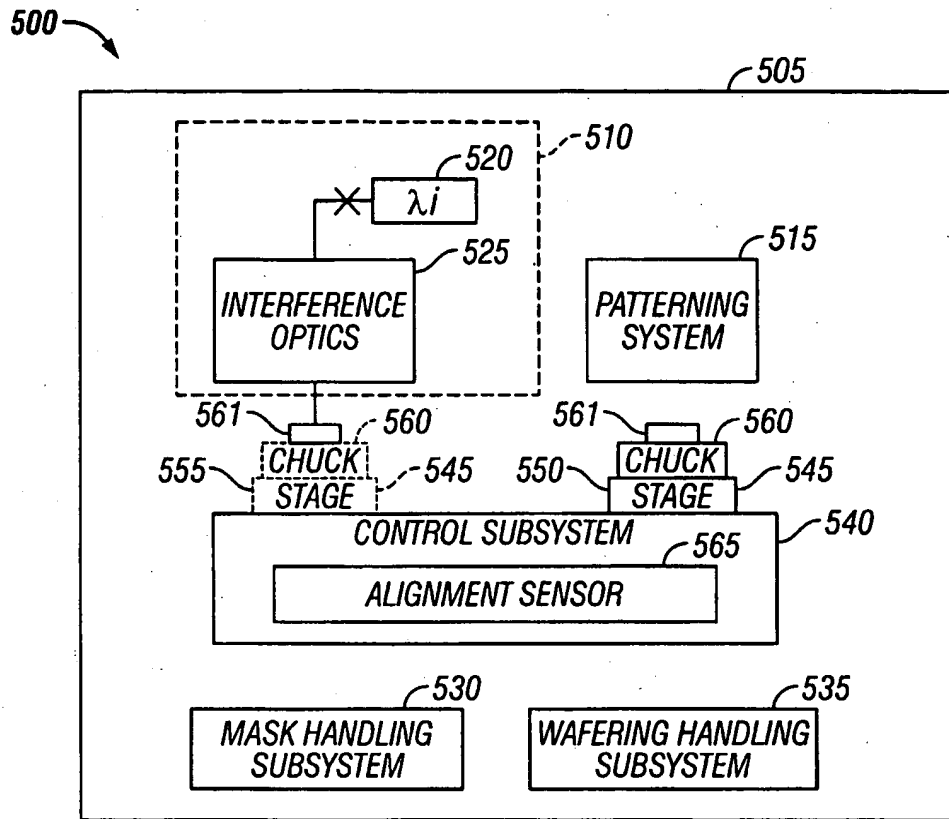


FIG. 5

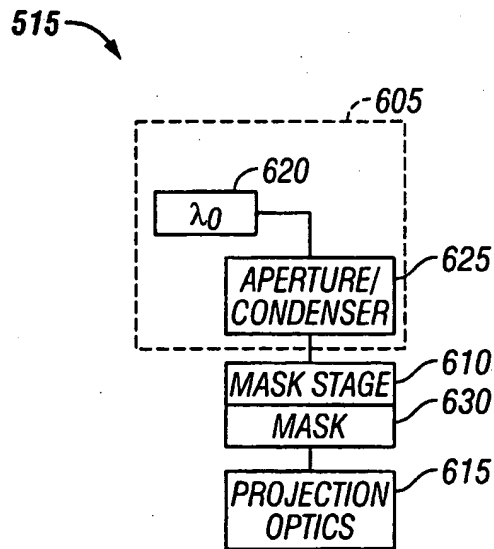


FIG. 6

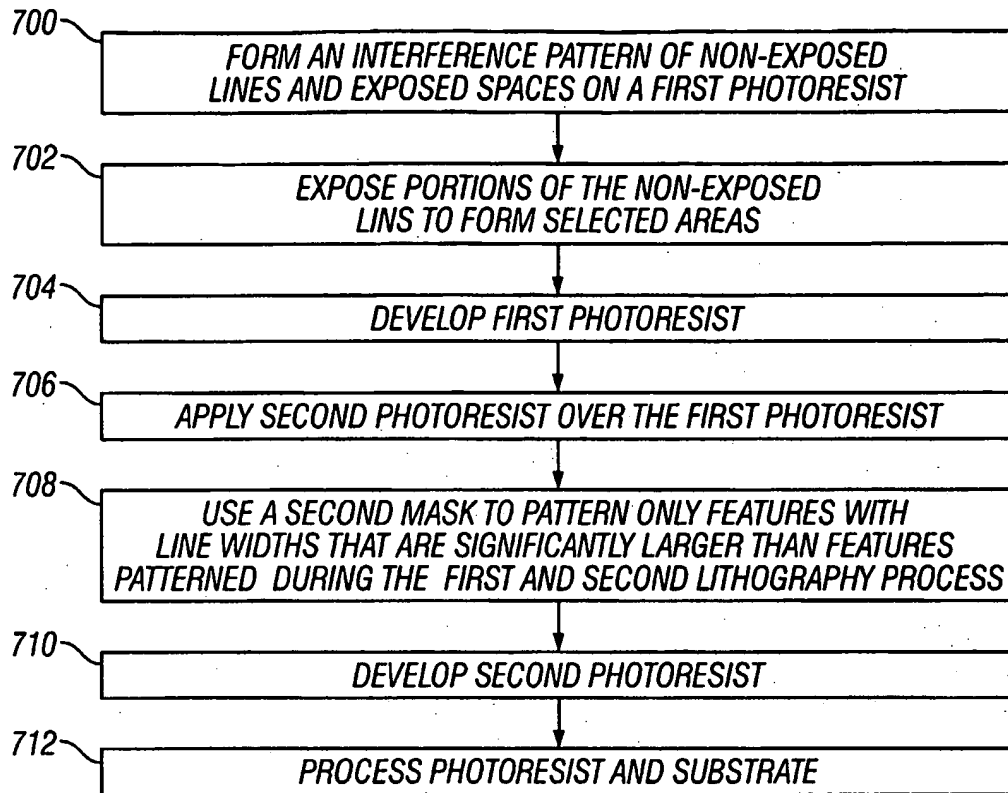


FIG. 7

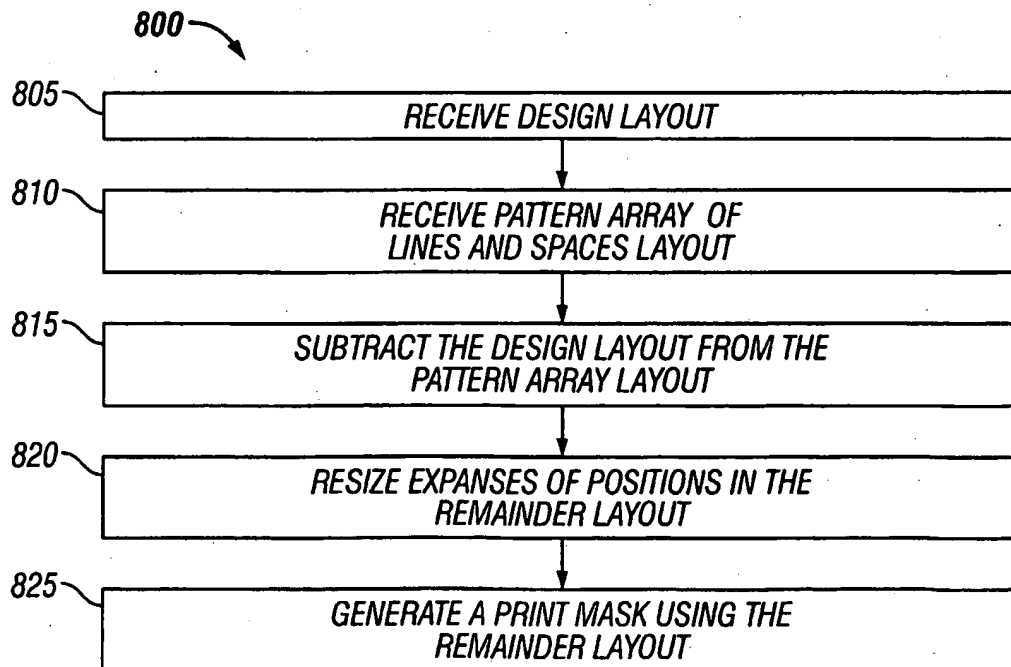


FIG. 8

900

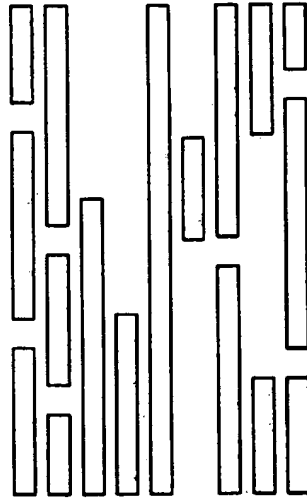


FIG. 9

1000

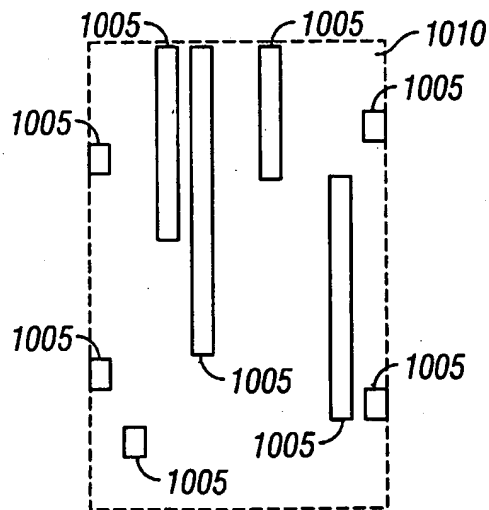


FIG. 10

1100

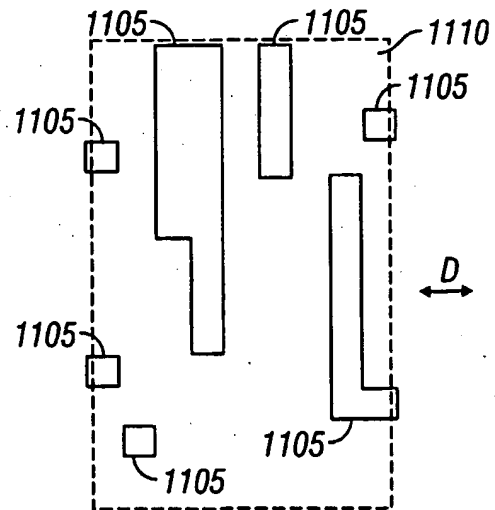


FIG. 11